Refine Search

Search Results -

Term	Documents
NEXT	1949139
NEXTS	52
SEQUENCE	1107473
SEQUENCES	282357
SECOND	5773035
SECONDS	533918
COUNT$3	0
COUNT	377754
COUNTA	115
COUNTABL	1
COUNTACC	1
(L20 AND (COUNT$3 OR INCREMENT$3 OR DECRMENT$3) NEAR8 (NEXT OR SUBSEQUENT$3 OR SEQUENCE OR SECOND OR ADJACENT$3)).PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD.	57

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Search: L21

Refine Search

Recall Text | Clear | Interrupt

Search History

DATE: Friday, August 20, 2004 Printable Copy Create Case

Set Name	Query	Hit Count	Set Name

h e b b cg b e e ch

side by side			result set
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L21	L20 and (count$3 or increment$3 or decrment$3) near8 (next or subsequent$3 or sequence or second or adjacent$3)	57	L21
L20	(fetch$6 or prefetch$5) and l2	99	L20
L19	prefetch$5 and l2	27	L19
L18	prefetch$5 and l1	1814	L18
DB=PGPB,USPT; PLUR=YES; OP=OR			
L17	l14 and l1	47	L17
L16	L14 and l2	0	L16
L15	L14 and l4	0	L15
L14	(711/123, 125, 219)![CCLS]	181	L14
L13	(711/23, 25, 219)![CCLS]	0	L13
L12	(711/23,25, 219)[CCLS]	0	L12
L11	L9 and l2	2	L11
L10	L9 and l3	2	L10
L9	(712/24, 207, 241, 248)![CCLS]	225	L9
L8	L5 and l4	30	L8
L7	L6 and l4	5	L7
L6	(711/123-221)![CCLS]	16611	L6
L5	(712/3-300)![CCLS]	10134	L5
DB=PGPB,USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR			
L4	L2 and (count$3 or increment$3 or decrment$3) near8 (next or subsequent$3 or sequence or second or adjacent$3)	68	L4
L3	L2 and (count$3 or increment$3 or decrment$3) near8 (next or subsequent$3 or sequence or second or adjacent$3 or preceed$3)	68	L3
L2	L1 near12 loop$4	122	L2
L1	(queu$3 or register$1 near2 file) near7 (instruction$1 or microinstruction$1)	8412	L1

END OF SEARCH HISTORY

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loop and queue and registers Search

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Results Key:
JNL = Journal or Magazine **CNF** = Conference **STD** = Standard

1 **Evaluating the use of register queues in software pipelined loops**
Tyson, G.S.; Smelyanskiy, M.; Davidson, E.S.;
Computers, IEEE Transactions on , Volume: 50 , Issue: 8 , Aug. 2001
Pages:769 - 783

[Abstract] [PDF Full-Text (3240 KB)] **IEEE JNL**

2 **Register queues: a new hardware/software approach to efficient software pipelining**
Smelyanskiy, M.; Tyson, G.S.; Davidson, E.S.;
Parallel Architectures and Compilation Techniques, 2000. Proceedings. International Conference on , 15-19 Oct. 2000
Pages:3 - 12

[Abstract] [PDF Full-Text (940 KB)] **IEEE CNF**

3 **Evaluating the use of register queues in software pipelined loops**
Tyson, G.S.; Smelyanskiy, M.; Davidson, E.S.;
Computers, IEEE Transactions on , Volume: 50 , Issue: 8 , Aug. 2001
Pages:769 - 783

[Abstract] [PDF Full-Text (3240 KB)] **IEEE JNL**

4 **Partitioned schedules for clustered VLIW architectures**
Fernandes, M.M.; Llosa, J.; Topham, N.;
Parallel Processing Symposium, 1998. 1998 IPPS/SPDP. Proceedings of the Fi Merged International...and Symposium on Parallel and Distributed Processing 1998 , 30 March-3 April 1998
Pages:386 - 391

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[Abstract] [PDF Full-Text (552 KB)] **IEEE CNF**

5 **A model for the high-level description and simulation of VLSI netwc**
van der Hoeven, A.J.; de Lange, A.A.J.; Deprettere, E.F.; Dewilde, P.M.;
Micro, IEEE , Volume: 10 , Issue: 4 , Aug. 1990
Pages:41 - 48

[Abstract] [PDF Full-Text (504 KB)] **IEEE JNL**

6 **A comparison of superscalar and decoupled access/execute architectures**
Farrens, M.K.; Ng, P.; Nico, P.;
Microarchitecture, 1993. Proceedings of the 26th Annual International Sympo on , 1-3 Dec. 1993
Pages:100 - 103

[Abstract] [PDF Full-Text (396 KB)] **IEEE CNF**

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